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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/772,986	01/31/2001	Hisao Hayashi	SON-2010	2637
7590 11/28/2007 RADER, FISHMAN & GRAUER, P.L.L.C			EXAMINER	
Suite 501			TRAN, THIEN F	
1233 20th Stree Washington, Do			ART UNIT	PAPER NUMBER
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			11/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

		Application No.	Applicant(s)
		09/772,986	HAYASHI ET AL.
	Office Action Summary	Examiner	Art Unit
		Thien F. Tran	2811
Danie d fe	The MAILING DATE of this communication app	ears on the cover sheet with the	correspondence address
WHIC - Exte after - If NC - Failu Any	ORTENED STATUTORY PERIOD FOR REPLY CHEVER IS LONGER, FROM THE MAILING DAY PERIOD FOR REPLY CHEVER IS LONGER, FROM THE MAILING DAY IN SIX (6) MONTHS from the mailing date of this communication. O period for reply is specified above, the maximum statutory period we are to reply within the set or extended period for reply will, by statute, reply received by the Office later than three months after the mailing ed patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be will apply and will expire SIX (6) MONTHS from the cause the application to become ABANDON	DN. timely filed m the mailing date of this communication. IED (35 U.S.C. § 133).
Status			
2a)⊠	Responsive to communication(s) filed on <u>08/28</u> This action is FINAL . 2b) This Since this application is in condition for allowar closed in accordance with the practice under E	action is non-final. nce except for formal matters, p	
Disposit	ion of Claims		•
5) <u></u> 6)⊠	Claim(s) 17-36 is/are pending in the application 4a) Of the above claim(s) is/are withdraw Claim(s) is/are allowed. Claim(s) 17-36 is/are rejected. Claim(s) is/are objected to. Claim(s) are subject to restriction and/or	vn from consideration.	•
Applicati	ion Papers	·	
10)	The specification is objected to by the Examiner The drawing(s) filed on is/are: a) acce Applicant may not request that any objection to the o Replacement drawing sheet(s) including the correcti The oath or declaration is objected to by the Examiner	epted or b) objected to by the drawing(s) be held in abeyance. So ion is required if the drawing(s) is o	ee 37 CFR 1.85(a). bjected to. See 37 CFR 1.121(d).
Priority ι	ınder 35 U.S.C. § 119	,	
a)l	Acknowledgment is made of a claim for foreign All b) Some * c) None of: 1. Certified copies of the priority documents 2. Certified copies of the priority documents 3. Copies of the certified copies of the prioric application from the International Bureau See the attached detailed Office action for a list of	s have been received. s have been received in Applica ity documents have been receiv (PCT Rule 17.2(a)).	tion No ved in this National Stage
Attachmen	• •		
2)	e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (PTO-948) mation Disclosure Statement(s) (PTO/SB/08) r No(s)/Mail Date	4) Interview Summar Paper No(s)/Mail [5) Notice of Informal 6) Other:	Date

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DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 17-27 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hisao et al. (JP 10-209467).

Hisao et al. discloses a thin film semiconductor device (Fig. 1) comprising: a gate electrode 5 in contact with an insulating substrate 1; a gate insulating film 4 in contact with a gate electrode, the gate electrode being between the insulating substrate and the gate insulating film. Hisao et al. further discloses the gate electrode 5 having an upper layer 5a of about 50-300 nm and a lower layer 5b of 50-200 nm (Hisao, paragraph 0012) that together provides a combined gate thickness of about 100-500 nm. The combined gate thickness with a lower limit range value of "about 100 nm" allows for values slightly below 100 nm. Hisao also discloses that the gate insulating film 4 has a thickness in the range of 100-200 nm which allows for a lower limit range value of 100 nm. As such, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to select the gate electrode 5 having a combined gate thickness slightly less than 100 nm and the gate insulating film 4 having a thickness of 100 nm to reduce the size of the device. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or

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workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. It is obvious that a selected thickness of the gate insulating film 4 of 100 nm is greater than a selected thickness of the gate electrode 5 of slightly below 100 nm as taught by Hisao. Also, it is noted that where claimed ranges overlap the ranges disclosed in the prior art, a prima facie case of obvious is established. See Woodruff, 919 F.2d at 1577, 16 USPQ2s at 1936, and In re Wertheim, 541 F.2d 257, 271, 191 USPQ 90, 103-04 (CCPA 1976).

Regarding claim 18, Hisao discloses a semiconductor thin film 2 in contact with the gate insulating film 4, the semiconductor thin film including a source region, a channel region, and a drain region.

Regarding claim 19, Hisao discloses a stopper 6 in contact with the channel region, the channel region being between the gate insulating film 4 and the stopper 6.

Regarding claim 20, the stopper is an insulator.

Regarding claim 21, the source and drain regions are adjacent said channel region.

Regarding claim 22, the gate electrode 5 includes a lower layer 5b and an upper layer 5a, the lower layer being between the insulating substrate and the upper layer.

Regarding claim 23, the lower layer 5b is in contact with the insulating substrate.

Regarding claim 24, the upper layer 5a is in contact with the lower layer.

Regarding claim 25, the gate insulating film 4 is between the upper layer 5a and the semiconductor thin film 2.

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Regarding claim 26, an electric resistance of said upper layer 5a is greater than said lower layer 5b, heat conductivity of said lower layer being greater than said upper layer (see paragraph 0012).

Regarding claim 27, the lower layer is a metallic material and said upper layer is another metallic material.

Regarding claim 36, Hisao discloses a display device (Fig. 6) comprising: a plurality of pixels 14 arranged in a matrix form, one of the plurality of pixels being driven by the thin film semiconductor device 3.

Claims 28-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hisao et al. (JP 10-209467) in view of Colgan et al. (US 5,912,506).

Hisao et al. as described above does not disclose the metallic material of the lower layer 5b contains aluminum and the upper layer 5a of molybdenum. However, aluminum and molybdenum are well known gate conductor materials as shown for example by Colgan. Colgan discloses a gate electrode comprising a lower layer 5 containing aluminum and an upper layer 7 of molybdenum (see Fig. 7). Therefore, forming the metallic material of the lower layer 5b containing aluminum and the upper layer of another metallic material, molybdenum (Mo) would have been obvious modification for the advantages that aluminum provides like high electrical conductivity and low cost; and the suppression of hillocks in the gate electrode due to the presence of the upper layer of molybdenum as taught by Colgan.

Regarding claims 29 and 30, Colgan discloses the metallic material being aluminum or an alloy of aluminum and silicon.

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Regarding claims 31-32, the another metallic material is molybdenum

Claims 31-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hisao et al. (JP 10-209467) in view of Seiki et al. (US 6,235,561).

Hisao et al. as described above does not disclose the metallic material of the lower layer 5b contains aluminum and the another metallic material of the upper layer 5a being formed of molybdenum, tantalum, tungsten or chromium. However, aluminum, molybdenum, tantalum, tungsten and chromium are well known gate conductor materials as shown for example by Seiki. Seiki discloses a gate electrode comprising a lower layer 111 containing aluminum and an upper layer 115 selected from the group consisting of chromium, tungsten, tantalum and molybdenum (see col. 1, lines 28-33; and col. 5, lines 49-52). Therefore, forming the metallic material of the lower layer 5b containing aluminum and the upper layer of another metallic material as claimed would have been obvious modification for the advantages that aluminum provides like high electrical conductivity and low cost; and the suppression of hillocks in the gate electrode due to the presence of the upper layer being selected from the group consisting of chromium, tungsten, tantalum, and molybdenum as taught by Seiki.

Response to Arguments

Applicant's arguments with respect to claims 17-36 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thien F. Tran whose telephone number is (571) 272-1665. The examiner can normally be reached on 6:30AM - 3:00PM Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

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Thien F Tran

Primary Examiner

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November 16, 2007